ABSTRACT OF THE DISCLOSURE

When an input address AD is previously stored in a register 211, if a matching signal EQ1 is active, then an address queue control circuit 19A latches an offset of the input address AD into a register 241, or else, latches the input address AD into a register 212 through a selector 262. When the input address AD is previously stored in the register 241, the address queue control circuit 19A latches the input address AD into the register 212 through the selector 262. After reading the contents of the register 211, the address queue control circuit 19A shifts the offset OFS of the register 241 to the offset field of the register 211 through a selector 261, and resets a valid flag EF of the register 241.